An 8-bit 100-GS/s Distributed DAC in 28-nm CMOS for Optical Communications

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Abstract—An 8-bit 100-GS/s digital-to-analog converter (DAC) using a distributed output topology in 28-nm low-power CMOS for optical communications is presented. The DAC can convert 1-kbyte design-for-test on-chip memory cyclically. By interleaving four 25-GS/s return-to-zero DACs, the highest signal frequency of the 100-GS/s DAC is about 25 GHz and the output image is located beyond 75 GHz. The 3-dB bandwidth exceeds 13 GHz at 100 GS/s. The effective number of bits and spurious-free dynamic range ranges from 5.3 bit and 41 dB to 3.2 bit and 27 dB from dc up to 24.9 GHz at 100 GS/s, respectively. Transmission rates of 120 and 45 Gb/s are obtained in an electrical and an optical back-to-back experiment, respectively. The DAC test chip consumes 2.5 W from a power supply with multiple outputs of 1.1, 1.5, and 2 V.

Index Terms—Digital–analog conversion, distributed amplifiers, filters.

I. INTRODUCTION

The optical coherent transceiver system is the common solution for optical communications with very high data rate [1]. A single carrier coherent optical transmitter is shown in Fig. 1. It employs four digital-to-analog converters (DACs) to generate two complex signals on both X- and Y-polarizations, respectively. The output of the DACs are linearly amplified to drive the optical modulators. The bandwidth and the resolution of the DACs are the keys to achieve higher data transmission rate and increase the utilization of the available spectrum.

Several high-speed DACs for this application are reported. A 6-bit 56-GS/s DAC in 65-nm CMOS is reported in [2]. An 8-bit DAC in 40 nm with a conversion rate up to 65 GS/s and 13-GHz bandwidth is announced in [3]. Another 6-bit return-to-zero DAC in 130-nm SiGe BiCMOS with up to a 50-GHz sampling clock and 4 $V_{pp}$ differential output swing is reported in [4] and it may directly drive the optical modulator. A SiGe DAC with 6 bits at 72 GS/s used in an arbitrary waveform generator (AWG) is reported in [5]. As the technology nodes scale down, DACs with even higher conversion rates will become feasible for next-generation optical transceivers with bit rates from 400 Gb/s to 1 Tb/s.

In CMOS DAC design, time interleaving is often used to achieve higher sampling rates [6], [7]. Several parallel DACs are connected to the output node, thus the output node suffers more parasitic capacitance than a non-time-interleaving DAC. At very high sampling rate, the output bandwidth is not more limited by the frequency response of the zeroth-order-hold output waveform, but is limited by the large parasitic capacitance. To overcome this problem, we use a distributed topology at the output stage of the proposed DAC. Similar as with the distributed amplifier, the large capacitance at the output node is distributed on the output transmission line and the output impedance is relatively constant over a large frequency range, and hence, the output bandwidth can be improved significantly.

Besides the analog output bandwidth, the image frequencies of the DACs also limit the usable signal bandwidth. The output signal can be oversampled to locate the image band far away from the signal band. The proposed DAC uses an image frequency suppression technique similar as in [8]. Two non-return-to-zero (NRZ)-sub-DACs clocked with 90° phase-shifted clocks combine their outputs as shown in Fig. 2. In the frequency domain, the signal components of the two NRZ-sub-DACs are in phase in the first Nyquist band, while the image frequency components in the second Nyquist band are in opposite phase. The sum of the two outputs has therefore no images in the second and the third Nyquist band of the NRZ-sub-DACs. The spectrum of the whole DAC is similarly as that of a DAC with 2x oversampling. However, the output zero frequency is still located at the sampling frequency $f_{SA} = n f_{S}$.

Each NRZ-sub-DAC consists of two time-interleaved (TI) RZ-sub-DACs. With this structure the NRZ-sub-DACs can convert at both positive

Fig. 1. Polarization-multiplexed square QAM optical transmission system.
This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

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Fig. 2. Circuit and interleaving concept of the proposed DAC and the principle of image frequency suppressing technique to shift the image frequency to a higher frequency band.

and negative clock level, thus it doubles the conversion rate to $f_{\text{in-sub}} = 2 \times f_{\text{c clk}}$. In the time domain, the outputs of the two NRZ-sub-DACs are skewed with half of the sampling period (180°). The sum of both outputs have effectively two times the conversion rate of the NRZ-sub-DAC ($2 \times f_{\text{s _ sub}}$). The overall conversion rate of the whole DAC is therefore $4 \times f_{\text{c clk}}$.

This paper presents a 100-GS/s 8-bit DAC in 28-nm low-power CMOS using the structure as shown in Fig. 2. In addition to the topics covered in [9], this paper presents a thorough analysis of circuit design, especially the design of the distributed DAC output stage, the design of the inductors, the timing alignment, and the phase detection. It also contains new measurement results with improved output bandwidth and conversion rate. An optical back-to-back communication experiment is also shown. Section II describes the DAC design. Section III shows the design of the distributed output stage. The measurement setup and measurement results are presented in Section IV, followed by conclusions in Section V.

II. DAC DESIGN

The DAC output stage is shown in Fig. 3. The architecture of the NRZ-sub-DAC output stage is similar as in [6]. Each RZ-sub-sub-DAC is segmented in 15 unary weighted current cells for the four most significant bits (MSBs) and four binary weighted current cells for the four least significant bits (LSBs). Although the current cells are segmented, the RZ-sub-sub-DACs are still controlled with binary code. The table in Fig. 3 shows the mapping between binary bit and the current cells that connected to each binary bit. Such mapping is called “pseudo encode” in [6]. To minimize the gradient error on chip, the current cells are placed in an interdigitated style. The four LSB current cells are placed in the middle and the unary current cells controlled by each MSB are placed symmetrical to the middle. The two RZ-sub-sub-DACs in one NRZ-sub-DAC output stage are also laid out in an interdigitated structure to improve matching. The current cells use cascode current sources with 1.8-V thick oxide MOSFETs to provide sufficient output impedance for 8-bit resolution. The clock switches switch the current to the analog output at the clock high level and to the dummy output at the clock low level in an alternating manner within one clock period. Since the two RZ-sub-sub-DACs are clocked with complimentary phase, the input data will be converted to the analog output at both high and low levels of the clock. This structure doubles the conversion rate of one NRZ-sub-DAC to two times the clock frequency.

The outputs of the current cells are connected to the output artificial transmission lines. The output artificial transmission lines are matched to 50Ω and consist of 16 segments. Each segment is connected to the outputs of four unary current cells on both sides. All the binary current cells are tied to one line segment. The left ends of the output lines are terminated with on-chip 50-Ω resistors. The right ends of the output lines are the analog outputs and are terminated off-chip with 50Ω. The signals from all current cell output must arrive at the analog output simultaneously for correct analog signal reconstruction. For a conventional DAC without an artificial transmission line at a relatively low sampling rate, the signal delay on the output line can be neglected. For the proposed distributed DAC with artificial transmission lines at a very high sampling rate, the signal delay on the output line cannot be neglected. Thus, the delay on the clock lines must match that on the output lines. The clock lines are also terminated at both ends with the proper resistance.
The architecture of the whole DAC test chip is shown in Fig. 4. The test chip has two identical NRZ-sub-DAC blocks. Each NRZ-sub-DAC block contains a 512-byte static RAM (SRAM) memory, a two-stage multiplexer (MUX) array, a distributed NRZ-sub-DAC output stage, and a clock divider.

The two memory blocks can store 1-kbyte data in total, i.e., 1-k symbols for an 8-bit DAC. The memory can be switched between “write” mode and “read” mode by an external signal. In the “write” mode, the memory can be written through a serial interface at a slow data rate. After the memory is fully programmed, it can be switched to the “read” mode. In the “read” mode, the data can be cyclically read out with a clock frequency synchronized to the DAC clock and be fed to the DAC output stage. Different possible signal waveforms including sinus waves, pulse amplitude modulated signals, and orthogonal frequency-division multiplexing (OFDM) signals can be easily generated and written to the memory to test the DAC performance up to 100 GS/s.

In the 100-GS/s read mode, the memory generates four 8.625 Gb/s data streams for each RZ-sub-sub-DAC. The pseudoencoders route 4-MSB input signals to 15 output signals to drive the correspondent current cells. The 4 LSBs are just delayed to match the timing of the pseudodecoder. These data streams are combined to one 19-b data stream through a two-stage MUX array, thus the data rate is increased from 6.25 Gb/s/channel to 25 Gb/s/channel. The 4:2 MUXs.

The timing between the data and clock input of the DAC output stage can be aligned using the circuit shown in Fig. 5(a), similar as in [7]. A 5-bit phase rotator is used to tune the phase of the data inputs. The correct data and clock phase is detected with a phase detector. The schematic and the timing diagram of the phase detector are shown in Fig. 5(b) and (c), respectively. When \( PD_{\text{out}} \) switches from high (H) to low (L), the timing is optimized: The H-level of the clock, which outputs the current steered by \( D_{\text{in}} \), is then located in the second half of the \( D_{\text{in}} \)-eye, when \( D_{\text{in}} \) has settled. The timing alignment circuits are implemented in both NRZ-sub-DAC output stages and can be tuned individually to ensure overall timing alignment. The timing alignment circuits with a two-phase selection (0° and 90°) capability are also implemented in the 8:4 MUX clock and memory clock path to ensure correct timing. The \( PD_{\text{out}} \) from each timing alignment circuit can be switched to an output pad using an internal control register. With an external evaluation program, the timing optimization process can be done automatically.

### III. Design of the Distributed Output Stage

The output bandwidth of a DAC is limited by several factors. The sinc function frequency response of an ideal staircase output NRZ DAC limits the DAC output spectrum and cause an amplitude roll-off of about 3.9 dB at the Nyquist frequency. The large parasitic capacitance of the output stage transistors and the output interconnect wiring further increase the amplitude roll-off. At very high frequency, the parasitic capacitances becomes the main factor that contributes to the amplitude attenuation. Reducing the parasitic capacitance requires smaller switching transistors and smaller interconnection area of the output stage. While the switching transistors are getting smaller with technology scaling, the area of the current source transistors does not change much. That is because of the limitations of mismatch and required voltage headroom. For the current sources, we use thick oxide MOSFETs to allow for more voltage drop and to achieve the matching requirements. The cascode structure ensures a sufficient high output impedance. Since the current source transistors are much larger than the switching transistors, the area of the DAC output stage is determined by the current sources. The area of the DAC core does not change much with the technology scaling, thus the parasitic capacitances on the interconnections are not reduced. The analog performance of the metal are even worse with the technology
Fig. 6. (a) Simplified single-ended schematic of the output stage. (b) Single-ended equivalent circuit the output line segment without losses. (c) Circuit model of the inductor. (d) Layout of the inductor.

scaling because the metal layer are thinner and are closer to substrate, which means the resistance and the parasitic capacitance became larger.

To increase the output bandwidth, the well-known distributed amplifier technique with artificial transmission lines is used in the presented DAC output stage. The output capacitance of the current switch is part of the line capacitance of the artificial transmission line. Thus the classic $RC$ limit of a lumped output stage can be exceeded. The benefit of the distributed structure is that the output and the input impedance can be kept constant over a wider frequency range, and hence, the output bandwidth can be increased. Each single-ended output line is divided into 16 segments; each line segment is connected to four current cell outputs on both sides, as shown in Fig. 6(a). The single-ended equivalent circuit without losses is shown in Fig. 6(b). The line impedance $Z_{\text{Lout}}$ is matched to $R_{\text{Lout}} = 50\,\Omega$. For a lossless line, the line impedance can be estimated with (1). The delay of the output line segment is given by (2). The clock line connected to the gate can have different line impedance, but the delay on the clock line must match the output line delay.

$$Z_{\text{Lout}} = \frac{L_{\text{out}}}{C_{\text{pL}} + 4 \times C_{\text{pout}}}$$

$$\tau_{\text{out}} = \sqrt{L_{\text{out}} \cdot (C_{\text{pL}} + 4 \times C_{\text{pout}})}$$

The output capacitance of the individual current cells varies with the voltages applied to the gate and drain of the switch transistor, i.e., the voltage of clock and the input data code. Therefore, we use the mean value of the capacitance for designing the artificial transmission line.

The artificial transmission line segments are built with on-chip spiral inductors to save chip area while implementing the required inductance. The circuit model and the layout of the inductor is shown in Fig. 6(c) and (d), respectively. The coarse parameters of the inductor can be calculated using the method described in [10], and then the exact parameters are optimized to fit the simulated S-parameters using an electromagnetic field simulator. The inductor layout is changed to achieve the 50-$\Omega$ line impedance using several iterative steps. The capacitance of the gate has a similar value as the drain capacitance, therefore we can use inductors with similar layout for clock and output transmission lines to match the delay to these lines.

Due to the series resistance of the output artificial transmission line, the resistance to the output pads decreases with decreased distance to the output pads. This systematic error would cause a large nonlinearity. Thus, the unary current cells of each NRZ-sub-DAC output stage are placed symmetric to the center of the transmission line. With proper placement, a binary coded structure provides better linearity than a thermometer coded structure.

The input data coming out of the MUX array is resampled by the clock coming out of the artificial clock transmission lines inside the current switch. Therefore, the MUX array output signals must also be aligned to the delay of the clock line. Additional delays for the input data signals are generated with delay buffers. The timing diagram between the DAC clock and DAC input data signals is illustrated in Fig. 7. Without the delay buffers, the sampling phase of the clock moves to the transition area of the data eye, thus causing errors at the output. With the delay buffers, the input data signals will be delayed to match the clock delay, and the sampling phase of the clock will stay in the stable area of the input data eye.

Fig. 7. Timing alignment of data input signals to DAC clock line.
IV. DAC MEASUREMENT

A. Electrical Measurement

The DAC test chip is designed and fabricated in a low-power 28-nm CMOS technology. Fig. 8(a) shows the chip micrograph and Fig. 8(b) shows the micrograph of the distributed DAC output stage with the layout dimensions indicated. The DAC test chip occupies 1.6 × 0.9 mm² and the distributed DAC output stage occupies 0.36 × 0.12 mm².

The DAC test chip is bonded and mounted on an RF test board shown in Fig. 9(b). The analog output can be directly probed with 40-GHz-bandwidth on-wafer-probes or bonded onto the RF printed circuit board (PCB). The two single-ended outputs are directly measured with a subsampling oscilloscope with 65-GHz bandwidth, as shown in Fig. 9(a).

A phase reference module is used to minimize jitter. The two single-ended clocks with 90° phase shift are generated by a signal generator. The 90° phase difference is adjusted with a mechanical phase shifter. The on-chip memory is programmed using an external program device based on a single-board PC with general-purpose input/output (GPIO) and a level-down shifter to output the proper logic levels. The signal measured by the subsampling oscilloscope is stored in a PC via a general-purpose interface bus (GPIB) and further analyzed with MATLAB.

The highest signal tone of a single 50-GS/s NRZ-sub-DAC in the first Nyquist-band is at 24.90234375 GHz. The period time of 1-k samples of the whole DAC is 10.24 ns. Depending on the phase shift of the input clock, the whole DAC can operate in two modes: (50 GS/s mode and 100 GS/s mode). For both NRZ-sub-DACs operating in phase (50 GS/s mode) and 180° out of phase (100 GS/s mode), the differential output captured by the oscilloscope and the corresponding spectra are shown in Fig. 10(a) and (b), respectively. The image frequency component can be suppressed by 45 dB in the 100 GS/s mode. Single samples of the 24.9-GHz output at 100 GS/s are shown in Fig. 10(c).

To determine the frequency-domain performance including effective number of bits (ENOB), spurious-free dynamic range (SFDR), and amplitude roll-off, the DAC output signals are probed with on-wafer probes and are 4× oversampled and averaged over 16 samples by the subsampling oscilloscope. The data is stored on a PC and processed with a 4-k fast Fourier transform (FFT) using MATLAB. To show the conversion rate flexibility, the ENOB and SFDR at 100 and 80 GS/s are shown in Fig. 11(a). All the frequency components up to half the sampling frequency (50 and 40 GHz, respectively) are included in the SFDR/ENOB calculation. At both conversion rates, the ENOB is 5.3 bit at dc and reduces to 3.2 bit up to the maximum frequency (24.9 and 19.9 GHz, respectively). The SFDR at both conversion rates is 41 and 37 dB at dc, respectively, and reduces to 27 dB up to the maximum frequency. To measure a single NRZ-sub-DAC, one of both NRZ-sub-DACs is “switched off” by outputting a constant value. The measured ENOB and SFDR at 50 and 40 GS/s are shown in Fig. 11(b). All the frequency components up to the Nyquist frequency (25 and 20 GHz, respectively) are included.
in the calculation. At 40 GS/s, the ENOB and SFDR achieves 5.9 bit and 45 dB at dc and reduce to 3.8 bit and 33 dB up to the Nyquist frequency (20 GHz), respectively. Both values become lower at 50 GS/s.

The 3-dB analog output bandwidth—including the roll-off due to the near-staircase-output of the NRZ-sub-DACs—is 10 and 9.2 GHz at 100 and 80 GS/s, respectively (Fig. 12). Considering the loss of the on-wafer probes and the cable connected to the sampling oscilloscope, the bandwidth of the DAC at the output pad is about 13 GHz at 100 GS/s, which is very similar to the simulation results with extracted parasitic elements, and is larger than that reported in [9]. The relatively large difference between the schematic and extracted simulation is due to an underestimate of the parasitic wiring capacitance when designing the artificial transmission line.

The time-domain characteristics are examined with pulse amplitude modulated signals using only one NRZ-sub-DAC. Fig. 13(a)–(c) shows the 512 random-symbol pulse-amplitude-modulation (PAM)2, PAM4 and PAM8 eyes measured with on-wafer probes without pre-emphasis (left) and with 10% digital pre-emphasis using one post tap (right) at 40 GS/s. In the case with pre-emphasis, the eyes are well opened for all pulse amplitude modulation schemes. At 50 GS/s, a very clear opened PAM4 eye can be observed in Fig. 13(d) even with the DAC outputs bonded on the PCB. These electrical back-to-back measurements show a transmission rate of up to 120 Gb/s (PAM8 at 40 GS/s) with the DAC test chip.

B. Optical Back-to-Back Experiment

The DAC application performance is tested in a single-polarization single-carrier optical back-to-back experiment. The single-ended DAC output is connected to a linear amplifier to drive the optical modulator as shown in Fig. 14(a). The optical signal is amplified with an optical amplifier and is converted to electrical signal with a photodiode. The output of the photodiode is measured either with a 50-GS/s real-time oscilloscope or with an 80-GHz bandwidth subsampling oscilloscope.
For this experiment, only one NRZ-sub-DAC is used while the other NRZ-sub-DAC is “switched off.” The conversion rate is limited to 30 GS/s because of the limited sampling rate of the real-time oscilloscope. The captured eye diagrams of PAM2, PAM3, and PAM4 with digital pre-emphasis at 30 Gbaud using the sampling oscilloscope are shown in Fig. 14(b). The transmitted data modulated with PAM2, PAM3, and PAM4 without pre-emphasis are captured with the real-time oscilloscope; the received data is post processed with a digital filter using MATLAB and the bit error rates (BERs) are evaluated. With PAM2 and PAM3, the transmitted data are received correctly, and with PAM4, the BER is 1.06E-3, i.e., a transmission rate up to 45 Gb/s (PAM3 at 30 Gbaud) can be achieved.

V. CONCLUSION

An 8-bit 100-GS/s DAC in 28-nm low-power CMOS for optical communication has been presented. The DAC uses an image frequency suppression technique to locate the image band far away from signal band, and therefore it is best suited for frequency-domain modulation schemes like OFDM. The ENOB and SFDR range from 5.3 bit and 41 dB to 3.2 bit and 27 dB for signal frequencies up to 24.9 GHz at 100 GS/s. The 3-dB output bandwidth is larger than 13 GHz with cable and probe deembedded. An electrical back-to-back transmission rate of 120 Gb/s and an optical back-to-back transmission rate of 45 Gb/s is obtained. Table I lists state-of-the-art high-speed DACs with conversion rates of 50 GS/s and above. To the best knowledge of the authors, the presented electronic DAC exhibits the largest conversion rate published up until now.

TABLE I

| TABLE I |

| STATE-OF-THE-ART HIGH-SPEED DAC |

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*) at -6 dBFS

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