Real-time 93.8-Gb/s polarization-multiplexed OFDM transmitter with 1024-point IFFT

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Abstract: We demonstrate a 93.8-Gb/s real-time optical OFDM transmitter with 1024-point IFFT using polarization-multiplexing and 4-QAM modulation. This is the highest IFFT size implemented for OFDM to our knowledge. The limited resources of FPGA make it challenging to place and route such a high size IFFT. The implementation penalty of the real time transmitter compared to the case where FPGAs are used as an arbitrary waveform generators increases up to 2 dB for BER of 7×10^{-4}. An optical back-back measurement showed required OSNR of 26.5 dB for a BER of 10^{-3}.

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1. Introduction

Coherent orthogonal frequency division multiplexing (CO-OFDM) offers all advantages of coherent detected modulation formats, such as dispersion un-managed transmission and electronic compensation of polarization-mode dispersion [1–3]. In addition, CO-OFDM is

highly suitable for the implementation of flexi-rate transponder technology, i.e. the ability to switch between modulation formats depending on the physical infrastructure. In next-generation transmission systems this is particularly important to find the optimum balance between maximum transmission reach and maximum feasible spectral efficiency. The negligible out-of-band signal power [3] of CO-OFDM makes it possible to multiplex multiple channels or sub bands with only small frequency spacing. Several experiments have been reported showing the generation of multi-band channels using CO-OFDM, realizing up to 1 Tb/s super-WDM channels for long-haul transmission systems [1,2]. This indicates that CO-OFDM is an ideal candidate for next-generation 400G/1T transmission.

Real-time OFDM implementations have attracted significant attention since it is essential to understand the limits of realistic digital signal processing (DSP) algorithms. In particular, a high inverse fast fourier transform (IFFT) size is required in order to keep the overhead for cyclic prefix at a minimum, i.e. for the same amount of chromatic dispersion compensation the cyclic prefix overhead increases as IFFT size decreases. In addition, a high FFT size provides a clear separation of the OFDM signal and radio frequency (RF) pilot used for laser phase noise compensation [4]. Table 1 summarizes recent real time OFDM transmitter achievements.

Table 1. Some Recent Real Time Transmitter Work

Ref	Bandwidth (GHz)	Data Rate (Gb/s)	IFFT size	Cyclic Prefix
[5]	4.2	8.4	128	0
[6]	6.3	12.1	256	8
[7]	1.9	11.3	32	8
[8]	25.4	101.5	64	0
[9]	11.9	23.9	1024	64
This Work	23.4	93.8	1024	64

Recently, we have reported a real-time CO-OFDM transmitter that utilizes 1024 point IFFT and polarization multiplexing with a nominal data rate of 93.8 Gb/s [10]. In this paper, we expand this work by explaining the effect of the pulse width offset of digital-to-analog converter (DAC) clock on optical signal-to-noise ratio (OSNR) performance.

2. Experimental setup

Figure 1 illustrates the electrical and optical blocks of the setup used to measure optical back-to-back performance of the real-time transmitter. The real time transmitter composed of two field programmable gate arrays (FPGA) is followed by DACs. The DAC outputs are amplified and fed to an IQ modulator. Polarization multiplexing is emulated by the use of a one symbol delay and a polarization beam splitter. At the receiver, coherent detection is realized with a polarization diverse 90 degrees hybrid and single ended photodiodes. After coherent detection offline processing is used including laser phase noise equalization, synchronization, and channel equalization with training symbols [3]. The laser used at the transmitter and receiver are external cavity laser (ECL) with a linewidth of ~100 kHz.

In the real time transmitter, the processing of the 1024-point FFT is realized with two synchronized FPGA, Xilinx ML525, boards. Each ML525 board is connected to a high speed DAC using 24 differential connections at 6.25 Gb/s each. On the DAC board, four groups of 6 bit data streams are built from the 24 inputs and then 4:1 multiplexed in order to form an output of 25 GS/s at 6-bit vertical resolution. The DAC boards are fed with a 12.5 GHz clock. One of the DACs provides a reference clock at 195.3 MHz to the two FPGA boards. The data is quadrature amplitude modulation (QAM) mapped and a gap of 20 subcarriers is inserted in the middle of the spectrum for RF-pilot laser phase noise compensation [4]. The payload is concatenated with the training symbols whose peak-to-average power ratios (PAPR) is minimized so that nonlinearities do not degrade the performance of channel equalization at the receiver. The digital signal processing in the real time transmitter is depicted in Fig. 1. Initially the QAM mapped bits are prepared for the complex IFFT. This preprocessing allows using one complex IFFT as two real valued IFFTs. Consequently the processing speed of the FPGA can be reduced to half [9]. After the IFFT, data stream is clipped, and cyclic prefix is

added. The real and imaginary parts are reorganized in a deinterleaving block in order to get a real output stream for DACs. Finally, the parallel data streams are multiplexed together into 24 channels that are sent to the FPGA outputs.
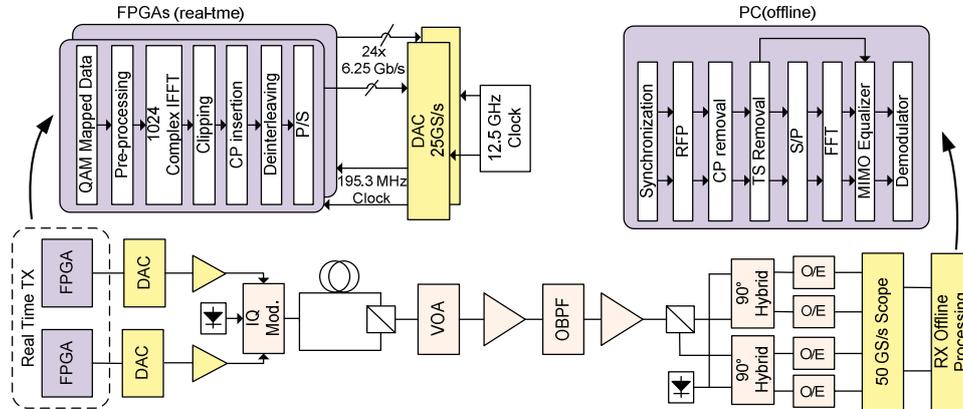

Fig. 1. Experimental setup including real time transmitter with FPGA and DAC boards, optical setup and offline processing blocks.

3. Results

A back-to-back performance evaluation was carried out in order to evaluate the performance of the real-time CO-OFDM transmitter. The following parameters were used; 960 subcarriers out of 1024 are 4 QAM modulated and 64 samples of cyclic prefix are added to each OFDM symbol in this experiment. 20 subcarriers in the middle of the spectrum are unmodulated in order to spare a gap for RF-pilot compensation. The rest of the subcarriers are used for oversampling. Two training symbols are sent every 40 payload symbols. Figure 2 shows the optical spectrum at the output of the polarization division multiplexed (PDM) OFDM signal. Aliasing products of the DAC are visible at both sides of the spectrum. Optionally low pass filters (LPF) can be used to eliminate these spectral components. Moreover, a pre-equalization function can improve the frequency roll-off of higher frequencies. The constellation diagram of the real-time transmitter at high OSNR is depicted in Fig. 3. In this constellation diagram is effected by residual laser phase noise and quantization noise. Figure 4 shows the OSNR performance. The real time transmitter is compared to the case where FPGA-DAC setup is utilized as an arbitrary waveform generator (AWG). For bit error ratio (BER) values of $5x10^{-3}$ and higher, a relatively small OSNR penalty of ~0.2 dB is observed between the real-time transmitter and the AWG. For lower BER values, the penalty of the real-time transmitter gradually increases up to approximately a 2dB difference for BER of $7x10^{-4}$ [10]. For all measured points a minimum of 2 million bits are evaluated

It is also found that the duty cycle error of the DAC clock input has an impact on performance. The DAC has a clock input of half of its sampling rate, in this case 12.5 GHz. Consequently, the DAC output is updated at both rising and falling edges of the clock signal. If there is an offset in pulse width of clock, the sampling would occur at $T_1, T_2, 2T_1 + T_2, 2T_1 + 2T_2,…$ where T_1 is $T-\Delta T$ and T_2 is $T + \Delta T$, T the is inverse of the sampling rate (F_s) and ΔT is duty cycle error. This would result in aliasing products at $m*F_s/2$ where m is a integer in the range of $-inf$ to $+ inf$ in addition to the regular aliasing products around F_s [11]. In case the modulated subcarriers exceed $F_s/2$, the interference products cannot be filtered out.
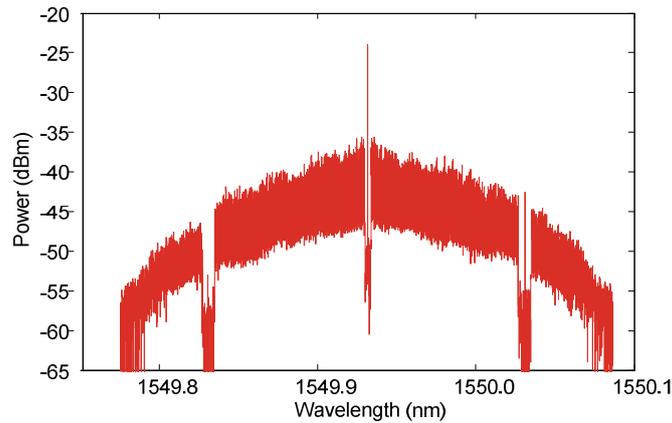
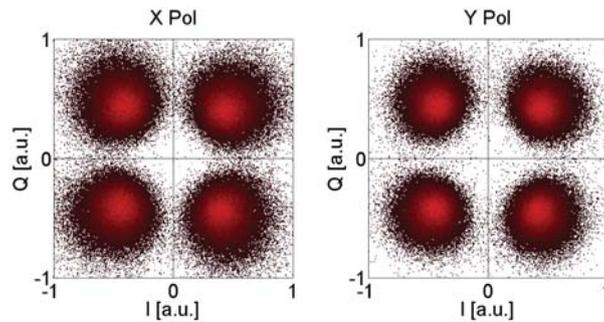Fig. 2. Optical spectrum of the 93.8-Gb/s OFDM signal.

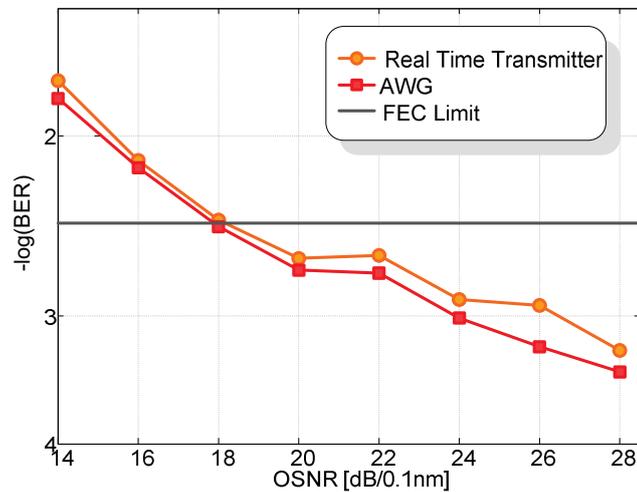Fig. 3. Constellation diagram of both polarizations at high OSNR.

Fig. 4. BER performance as a function of the OSNR.

A clock offset can be applied via DAC graphical user interface (GUI). The energy per symbol over noise spectral density (E_s/N_0) versus modulated subcarrier graphs are shown in Fig. 5 for the case of real output OFDM, i.e., discrete multitone modulation (DMT) [12]. For this measurement 900 subcarriers are modulated and measurements are taken electrical back-

to-back. Since real output OFDM is used, only one FPGA-DAC pair was sufficient. In DMT, half of the subcarriers are complex conjugate and flipped version of the other half so only one half of subcarriers are shown. Figure 5(a) shows the sudden drop due to the interference of aliasing products around $F_s/2$ when no clock offset is applied with the DAC GUI. Figure 5(b), on the other hand, is with clock offset and there is only frequency roll-off due to DACs. For this scenario, average E_s/N_0 increased 3 dB.
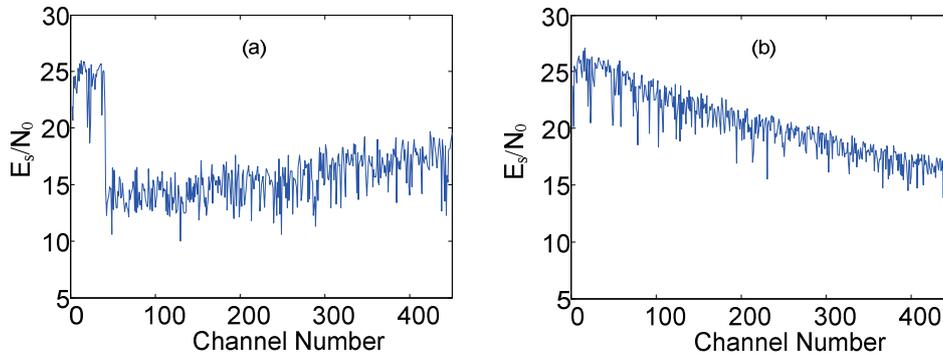
Fig. 5. E_s/N_0 vs. modulated subcarrier (a) without and (b) with clock offset for electrical back-to-back DMT where 900 subcarriers are modulated.

The OSNR performance in Fig. 4 was measured again with clock offset. A 0.5 dB improvement is obtained for BER of 10^{-3}.

4. Challenges of the 1024-point IFFT realization

The IFFT uses the decimation in time radix 2 algorithm and for the 1024-point implementation almost all resources of the FPGA are used. The DSP uses 82% of DSP48E, 28% of block random access memories (RAM), 85% slice registers and 72% slice look up tables, one phase locked loop and one digital clock manager. The excessive usage of the FPGA makes it challenging to place and route the code in the FPGA without any timing violations. Reference 9 shows the single polarization performance of the previous generation of DACs at 25 GS/s. The new generation of DACs used for this paper work in principle support sampling rates up to 30 GS/s. However, in this experiment the sampling rate was limited to 25 GS/s because of the limitations of the FPGAs. As a result of the excessive resource usage, the complete FPGA code drew 16 A of current at 25 GS/s. At such high current it is challenging to keep the internal voltage of FPGAs within the operating range ($0.9V < V_{int} < 1.1V$). At higher sampling rates a higher current would have been required which would lead to a too large voltage drop to the FPGA core in addition to a performance degradation caused by the fact that the FPGA boards heat up. In [9], where the data rate is much lower compared to [10] and hence this work, the penalty between the AWG and real time transmitter was negligible. On the other hand, in this paper, more subcarriers are modulated to achieve a higher data rate and some new functionalities are added such as the pseudorandom bit sequence (PRBS) scrambling, PRBS shifter, which are required for the synchronization for the new generation of DACs, and pre-processing function. Consequently, the resource limitations of the FPGA are pushed even further resulting in an increase of the real-time implementation penalty.

5. Conclusion

We successfully demonstrate a real time optical OFDM transmitter at 93.8 Gb/s with a 1024 point IFFT size and polarization multiplexing. Compared to an arbitrary waveform generator a significantly power increase is observed in the FPGA resulting in an OSNR penalty of up to 2 dB at a BER of $7x10^{-4}$. This clearly shows the challenges involved for the implementation of a real time 1024 point IFFT.