Clock Recovery with DGD-tolerant Phase Detector for CP-QPSK Receivers

C. Hebebrand[1], A. Napoli[2], A. Bianciotto[2], S. Calabro[2], B. Spinnler[2] and W. Rosenkranz[1]
[1]*Chair for Communications, University of Kiel, Kaiserstraße 2, D-24143 Kiel, Germany, E-mail: ch@tf.uni-kiel.de*
[2]*Nokia Siemens Networks, Broadband Connectivity Solutions, St.-Martin-Str. 76, 80240 München*

Abstract: We present three novel phase detector structures for a 112 Gbit/s CP-QPSK system, which provide, even in the presence of DGD, valid tracking information for a fully digital clock recovery.

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1. Introduction

Coherent polarization multiplexed (CP) QPSK is one of the most promising modulation formats for high-speed optical transmission. In coherent receivers the data recovery including the clock recovery is usually done in the digital domain. However in chromatic dispersion (CD) and differential group delay (DGD) limited systems, conventional phase error detectors like the Gardner phase detector [1, 2] may fail to provide valid tracking information to the clock recovery. This will happen especially when the signals on the two polarizations exhibit a delay of half a symbol duration against each other and equal power splitting within the two polarizations (i.e the polarization mixing angle equals approx. π/4). In this paper we present three DGD tolerant phase detector structures, which provide, even in presence of this propagation effect, valid tracking information to the clock recovery.

2. System setup and design of clock recovery with PLL and conventional Gardner phase detector

Fig. 1a shows a conventional digital clock recovery, which is implemented as a second order phase-locked loop (PLL) with an active PI-filter (i.e. a filter with perfect integrator path) and a Gardner phase detector (GPD) [1].

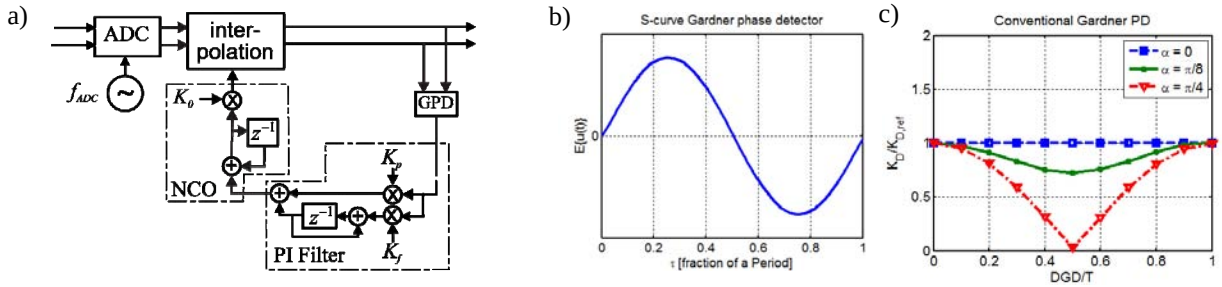

Fig. 1: a) Fully digital clock recovery, b) S-curve of the Gardner phase detector and c) normalized phase detector constant vs. DGD/T for various polarization mixing angles α for clock recovery with conventional Gardner PD.

The operating mode of the clock recovery is as follows: After the analog-to-digital converter (ADC) there are about two samples per symbol. The exact value depends on the difference between the clock frequency of the ADC and twice the symbol frequency of the received signal (here called symbol frequency offset Δf_{Sym}). To correct Δf_{Sym} and the initial phase shift of the ADC, the sampled signal is interpolated at the time instants $t + k\,T/2 + \varepsilon$ produced by the numerically controlled oscillator (NCO) of the digital PLL. The GPD uses three samples for calculation of the overall timing error [1, 2]. The S-curve of the GPD is shown in Fig. 1b.

In order to demonstrate the susceptibility of the pure Gardner phase detector to distortions, Fig. 1c depicts the normalized phase detector constant K_D vs. normalized differential group delay DGD/T for various polarization mixing angles α. $K_{D,ref}$ is defined as the K_D at DGD = 0T and $\alpha = 0$. The phase detector constant becomes about zero for DGD = 0.5 T and α = π/4 and thus no tracking information is available.

3. System setup and design of clock recovery with PLL and DGD tolerant phase detector

To avoid losing tracking information at the critical point DGD = 0.5 T and α = π/4 three DGD tolerant phase

detector structures are investigated. All three structures use the combination of the received signal on x- and y-polarization and two GPDs, the output of which are added on each polarization. In the first structure (Fig. 2a), the original received signal is processed, after the interpolation, by the first GPD, while the second GPD processes the interpolated and equalized signal, where the equalizer coefficients are optimized for the case DGD = 0.5 T and $\alpha = \pi/4$. This structure is hereafter referred to as "Structure Signal+DGD". In the second PD structure, here named "Structure withoutDGD" (Fig. 2b), the added signals on the x- and y-polarization, multiplied with 0.5, are processed by second GPD. Finally, the last structure (Fig. 2c) reproduces the one of Fig. 2a, with the difference that the x-polarization after the interpolator is delayed by half a symbol duration, which is equivalent to an equalization optimized for DGD = 0.5 T and $\alpha = 0$. This structure is referred to as "Structure onlyDGD".

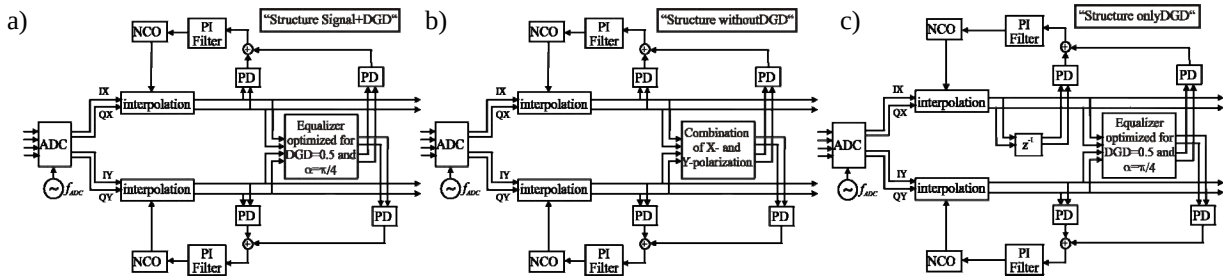

Fig. 2: a) "Structure Signal+DGD", b) "Structure withoutDGD" and c) "Structure onlyDGD"

Fig. 3 shows the normalized phase detector constant K_D vs. DGD/T for various polarization mixing angles α for the three PD structures exemplarily for the x-polarization. It can be seen that for all of them the phase detector constant remains larger than zero for all considered distortion scenarios, thus the tracking information is available. For the "Structure Signal+DGD" and "Structure onlyDGD", the phase detector constant K_D is stable for $\alpha = \pi/4$, due to the fact that for this case the combined PD output is influenced by almost only one single PD output. The combined output of the PD is influenced by both PDs and the value of the combined K_D depends on the phase shift and K_D of the S-curves of the respective GPDs.

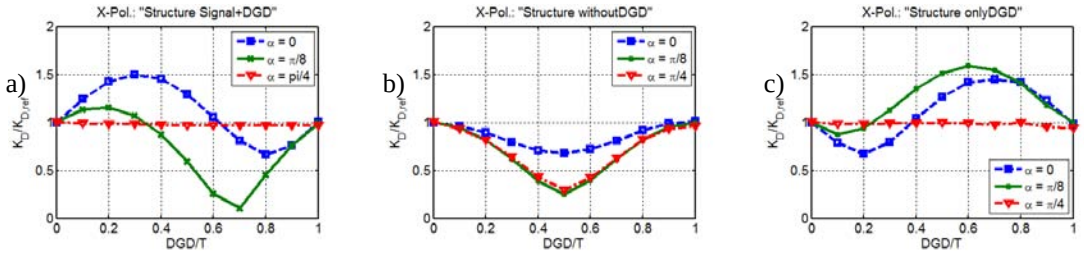

Fig. 3: $K_{D/}$ $K_{D,ref}$ vs. DGD/T ($K_{D,ref}$ is the K_D at DGD = 0T and $\alpha = 0$) for various polarization mixing angles α for a) "Structure Signal+DGD", b) "Structure withoutDGD" and c) "Structure onlyDGD"

We observe that with these proposed schemes, the S-curves of both outputs of the PDs are shifted against each other, so that the resulting S-curve is shifted compared to the one of a conventional GPD. Because of this the PLL will lock in a different point than the PLL with only a simple GPD. This results in a constant phase shift with respect to the optimum sampling point of the received signal at the output of the clock recovery, which has to be corrected by a following equalizer. The main task, however, i.e. the ability to correct the frequency offset of the ADC, is not affected by this.

4. Conclusion

We have presented three novel phase detector structures, which provide valid tracking information to the phase-locked loop even in the presence of DGD, so that the main task of correcting the symbol frequency offset of the ADC can be fulfilled.

5. References

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[2] F. M. Gardner, “Phaselock Techniques”, 2nd edition, Wiley, 1979