Digital Clock Recovery with Adaptive Loop Gain to Overcome Channel Impairments in 112 Gbit/s CP-QPSK Receivers

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Abstract *The effective loop parameters of digital PLL based clock recovery schemes vary with the degree of impairments in the received signal. We present a novel scheme that guarantees stable PLL design parameters independently of input signal distortions.*

Introduction

Recently, digital signal processing (DSP) in combination with coherent detection has received significant attention in high-speed optical transmission. Using this technique, realization of clock recovery, equalization and carrier recovery in the digital domain will be possible. The main task of the clock recovery is to provide a signal to the equalizer and carrier recovery subsystems, from which the jitter and the symbol clock frequency offset of the analog-to-digital converter (ADC) is removed. In a phase-locked loop (PLL) based clock recovery design, the phase detector (PD) constant (e.g. the slope of the S-curve) is an important parameter which has to be known[1,2] and which determines loop performance (e.g. bandwidth, stability) significantly. The PD constant K_D however depends on the received signal and may vary significantly during transmission e.g. due to differential group delay (DGD), chromatic dispersion (CD) or signal dynamics. In this paper, we present a clock recovery structure with an additional open loop configuration, which makes the design of a digital phase-locked loop independent of the slope of the phase detector due to a novel scheme with adaptive control of loop gain.

System setup and design

Fig. 1a shows a conventional digital clock recovery, which is implemented as a second order phase-locked loop (PLL) with an active PI-filter (i.e. a filter with perfect integrator path) and a Gardner phase detector (GPD)[3].

The operating mode of the clock recovery is as follows: The analog-to-digital converter (ADC) delivers approximately two samples per symbol. The exact value depends on the difference between the clock frequency of the ADC and twice the symbol frequency of the received signal (here called symbol frequency offset Δf_{Sym}). To correct Δf_{Sym} and the initial phase shift of the ADC, the sampled signal is interpolated at the time instants $t + k\ T_S/2 + \varepsilon$ produced by the numerically controlled oscillator (NCO) of the digital PLL. The GPD uses three samples for calculation of the overall timing error[2,3]. The S-curve of the GPD is shown in Fig. 1b.

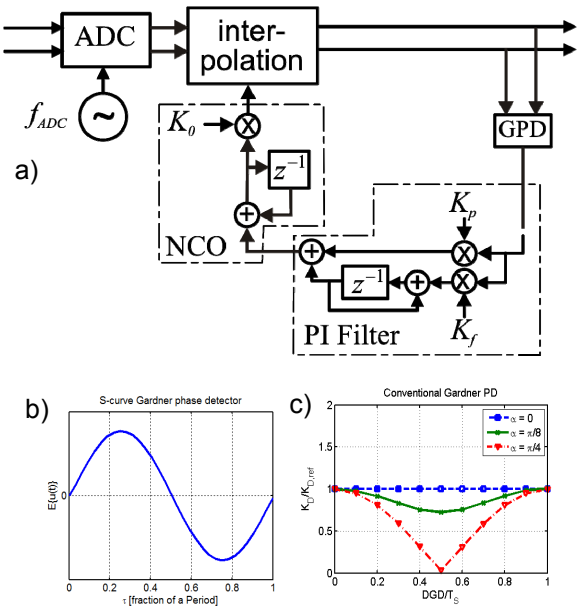

Fig. 1: a) Fully digital clock recovery, b) S-curve of the Gardner phase detector and c) normalized phase detector constant vs. DGD/T_S for various polarization mixing angles α for clock recovery with conventional Gardner PD.

In order to demonstrate the susceptibility of the pure Gardner phase detector to distortions, Fig. 1c depicts the normalized phase detector constant K_D vs. normalized differential group delay DGD/T_S for various polarization mixing

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angles α. $K_{D,ref}$ is defined as the K_D at DGD = 0T and α = 0.

Parameters of the PLL

To characterize a second order PLL, in principle only the damping factor ζ and either the natural frequency ω_n or the loop bandwidth B_L have to be known. From these all other parameters can be derived[1,2]:

$$\omega_n T_s = \sqrt{K_f K_D K_0}, \quad \zeta = \frac{1}{2}\sqrt{K_D K_0 \frac{K_p^2}{K_f}}, \qquad B_L T_s = \omega_n T_s \left(\zeta + \frac{1}{4\zeta}\right) \tag{1}$$

where K_p and K_f are the amplification factors of the PI-filter in the proportional- and integral part respectively (see Fig. 1a), K_0 is the oscillator constant, K_D is the phase detector constant and T_s is the symbol duration. The amplifications K_p, K_f and K_0 are fixed parameters, which will not change during transmission, whereas the parameter K_D depends mainly on the pulse shape and the power of the received signal but also on the distortions on the channel due to DGD and CD. Due to these distortions, K_D varies depending on the transmission conditions. Therefore, it has to be distinguished between $K_{D,design}$, which is used to design the PLL and $K_{D,signal}$ which results at the PD output after transmission. Simulations have shown that due to varying DGD on the channel the $K_{D,signal}$ at the PD output changes (Fig. 1c) and this changes the loop gain of the whole PLL. The impact of changing $K_{D,signal}$ on the parameters of the PLL can be seen in Equation (2). It gives the effective parameters for the case that $K_{D,design} = x\, K_{D,signal}$. For $K_{D,signal} < K_{D,design}$ the effective loop bandwidth $B_{L,eff}$ decreases due to the decreasing loop gain and vice versa.

$$\zeta_{eff} = \frac{1}{\sqrt{x}}\zeta_{design}, \quad \omega_{n,eff} = \frac{1}{\sqrt{x}}\omega_{n,design}, \qquad B_{L,eff} = z\, B_{L,design} \tag{2}$$

with

$$z = \left(1 + \frac{\zeta_{design}}{\zeta_{design} + \frac{1}{4\zeta_{design}}}\left(\frac{1}{x} - 1\right)\right) \tag{3}$$

This behaviour is a critical point in the design of the clock recovery. The clock recovery has to be stable during the entire transmission even if the loop gain changes. In general there are two limitations for the loop bandwidth $B_{L,eff}$. The first one is the maximum symbol frequency offset which can be tracked. This limitation can be overcome by use of an active PI-filter which guarantees, at least in theory, that arbitrarily large symbol frequency offsets Δf_{Sym} can be tracked. Thus, for the lower limit of the loop bandwidth only the pull-in time is a criterion. The second limitation is the additional delay in the loop. The maximum loop bandwidth for a given additional loop delay of M_{design} symbols can be calculated as follows[4]:

$$B_{L,design} T < 1/(2M_{design} + 1)\left(\zeta_{design} + \frac{1}{4\zeta_{design}}\right) \tag{4}$$

Now, if the effective loop bandwidth $B_{L,eff}$ increases, e.g. due to varying DGD, the PLL may become unstable. The effective maximum tolerable additional loop delay of M_{eff} symbols for $K_{D,design} = x\, K_{D,signal}$ is:

$$2M_{eff} + 1 = (2M_{design} + 1)\sqrt{x}. \tag{5}$$

Adaptive loop gain control

Fig. 2 shows our novel solution to overcome the problem of changing loop properties due to a varying $K_{D,signal}$.

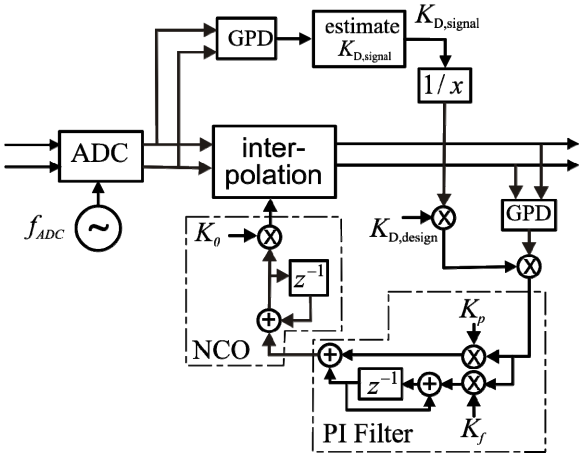

Fig. 2: Proposed clock recovery with novel adaptive control of loop gain

Before the clock recovery, an open loop configuration with the same PD as in the closed loop is implemented. The interpolator can be omitted for this structure if a symbol frequency offset is always present, which will be the case in realistic setups. In this open loop configuration first the S-curve is estimated and from this $K_{D,signal}$ is calculated. The inverse of the

calculated $K_{D,signal}$ is multiplied with $K_{D,design}$ and afterwards fed as an additional amplification or attenuation factor into the loop. The place of this additional multiplication can be everywhere in the loop. Due to this adaptive control the influence of $K_{D,signal}$ on the dynamics of the PLL is canceled out. The speed of this adaptive control depends on the symbol frequency offset of the ADC. This offset determines the time required to observe the full S-curve, which is necessary to determine the actual $K_{D,signal}$.

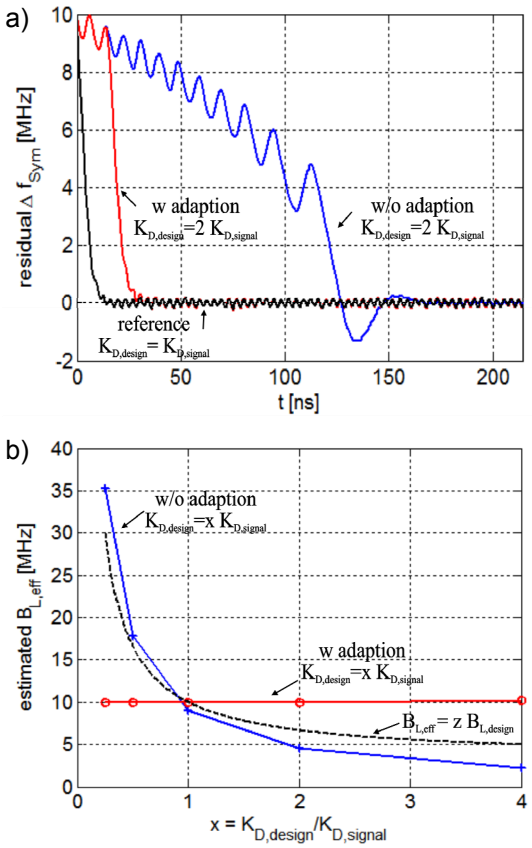

Fig. 3: a) Residual Δf_{Sym} during the lock-in procedure for a system with and without adaptive control with $K_{D,design} = 2\ K_{D,signal}$ and a reference system with $K_{D,design} = K_{D,signal}$ and b) estimated loop bandwidth $B_{L,eff}$ after PI-filter for both systems and $B_{L,eff} = z\ B_{L,design}$ (equation (2) and (3)) vs. x after lock-in of the PLL

As an example, Fig. 3a shows the residual symbol frequency offset Δf_{Sym}, derived from the output of the integral part of the PI-filter, during the lock-in procedure for a 112 Gbit/s CP-QPSK transmission with an OSNR of 15 dB. For the red (w adaption) and blue (w/o adaption) curve we assumed $K_{D,design} = 2\ K_{D,signal}$ and for the black (reference) curve $K_{D,design} = K_{D,signal}$. The symbol frequency offset was set to $\Delta f_{Sym} = 10$ MHz, the damping factor was $\zeta = 0.707$ and the loop bandwidth $B_{L,design} = 10$ MHz. The curve with adaptive control exhibits the same behaviour as the reference system after the time needed to calculate $K_{D,signal}$ (for this Δf_{Sym} about 11200 samples ~200 ns), whereas the system without adaptive control requires a much longer pull-in and lock-in time, which reveals a smaller loop bandwidth[2].

From the standard deviation of the output after the PI-filter the loop bandwidth $B_{L,eff}$ after lock-in of the PLL, for the system without and with adaptive control, was estimated for various values of the factor $x = K_{D,design}/K_{D,signal}$ (Fig. 3b). It can be seen that the estimated loop bandwidth of the system without adaptive control shows almost the same behaviour as the analytical curve for the effective loop bandwidth $B_{L,eff} = z\ B_{L,design}$ (equation (2) and (3), dashed curve in Fig. 3b). On the contrary the estimated loop bandwidth for the system with adaptive control is the same for all values of x, which implies a constant loop gain and according to this a design of the digital PLL which is independent of $K_{D,signal}$.

Conclusions

We have presented a novel approach for an adaptive control of the loop gain for a clock recovery subsystem based on a digital phase-locked loop. This adaptive control makes the design of the loop independent of the properties of the incoming signal. Without such a control the clock recovery may become unstable due to varying loop gain caused by distortions like chromatic dispersion or differential group delay.

References

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